What is claimed is:

1. An input/output circuit comprising:

a reference clock generator configured to generate a reference clock;

a signal transmitter configured to transmit serial data in synchronization with one of the reference clock and a test clock;

a signal-receiving circuit configured to receive the serial data, and to generate a converted signal from the serial data; and

a test circuit configured to detect an error between each phase of the converted signal and the test clock when the signal transmitter operates in synchronization with the test clock.

2. The input/output circuit of claim 1, wherein the test circuit comprises a test clock generator configured to generate the test clock.

3. The input/output circuit of claim 1, wherein the test circuit comprises a selector configured to supply one of the test clock and the reference clock to the signal transmitter.

4. The input/output circuit of claim 1, wherein the signal-receiving circuit comprises:

a receiver configured to buffer the serial data; and

a clock recovery circuit configured to generate a recovery clock as the converted signal, based on the buffered serial data and the reference clock.

5. The input/output circuit of claim 4, wherein the test circuit comprises a clock comparator configured to compare the recovery clock with the test clock.

6. The input/output circuit of claim 5, wherein the clock comparator comprises:

a plurality of delay circuits configured to generate a plurality of delay signals by delaying the recovery clock;

a plurality of latch circuits configured to generate a plurality of latch signals by latching the delay signals in synchronization with the test clock;

a plurality of EXOR circuits configured to generate a plurality of error detection signals by providing an EXOR operation to the latch signals; and

a plurality of counters configured to count the error detection signals in synchronization with the test clock.

7. The input/output circuit of claim 1, wherein the signal-receiving circuit comprises:

a receiver configured to buffer the serial data;

a clock recovery circuit configured to generate a recovery clock as the converted signal, based on the buffered serial data and the reference clock; and

a deserializer configured to convert the buffered serial data into parallel data in synchronization with the recovery clock, and to supply the parallel data as the converted signal to the test circuit.

8. The input/output circuit of claim 7, wherein the test circuit comprises a clock comparator configured to compare the parallel data with the test clock.

9. The input/output circuit of claim 8, wherein the clock comparator comprises:

a plurality of delay circuits configured to generate a plurality of delay signals by delaying the parallel data;

a plurality of latch circuits configured to generate a plurality of latch signals by latching the delay signals in synchronization with the test clock;

a plurality of EXOR circuits configured to generate a plurality of error detection signals by providing an EXOR operation to the latch signals; and

a plurality of counters configured to count the error detection signals in synchronization with the test clock.

10. A semiconductor integrated circuit comprising:

an input/output circuit configured to transmit serial data in synchronization with a test clock, and to generate a converted signal from the serial data, to detect an error between each phase of the converted signal and the test clock; and

an internal circuit configured to perform transmission and reception of signals to external circuits via the input/output circuit.

11. The semiconductor integrated circuit of claim 10, wherein the test clock is supplied by the internal circuit.

12. The semiconductor integrated circuit of claim 10, wherein the input/output circuit comprises:

a reference clock generator configured to generate a reference clock;

a signal transmitter configured to transmit the serial data in synchronization with one of the reference clock and the test clock;

a signal-receiving circuit configured to receive the serial data, and to generate the converted signal from the serial data in synchronization with the reference clock; and

a test circuit configured to detect the error when the signal transmitter operates in synchronization with the test clock.

13. The semiconductor integrated circuit of claim 12, wherein the test circuit comprises

a test clock generator configured to generate the test clock.

14. The semiconductor integrated circuit of claim 12, wherein the test circuit comprises a selector configured to supply one of the test clock and the reference clock to the signal transmitter.

15. The semiconductor integrated circuit of claim 12, wherein the signal-receiving circuit comprises:

a receiver configured to buffer the serial data; and

a clock recovery circuit configured to generate a recovery clock as the converted signal, based on the buffered serial data and the reference clock.

16. The semiconductor integrated circuit of claim 15, wherein the test circuit comprises a clock comparator configured to compare the recovery clock with the test clock.

17. The semiconductor integrated circuit of claim 16, wherein the clock comparator comprises:

a plurality of delay circuits configured to generate a plurality of delay signals by delaying the recovery clock;

a plurality of latch circuits configured to generate a plurality of latch signals by latching the delay signals in synchronization with the test clock;

a plurality of EXOR circuits configured to generate a plurality of error detection signals by providing an EXOR operation to the latch signals; and

a plurality of counters configured to count the error detection signals in synchronization with the test clock.

18. The semiconductor integrated circuit of claim 12, wherein the signal-receiving circuit comprises:

a receiver configured to buffer the serial data;

a clock recovery circuit configured to generate a recovery clock as the converted signal, based on the buffered serial data and the reference clock; and

a deserializer configured to convert the buffered serial data into parallel data in synchronization with the recovery clock, and to supply the parallel data as the converted signal to the test circuit.

19. The semiconductor integrated circuit of claim 18, wherein the test circuit comprises a clock comparator configured to compare the parallel data with the test clock.

20. The semiconductor integrated circuit of claim 19, wherein the clock comparator comprises:

a plurality of delay circuits configured to generate a plurality of delay signals by delaying the parallel data;

a plurality of latch circuits configured to generate a plurality of latch signals by latching the delay signals in synchronization with the test clock;

a plurality of EXOR circuits configured to generate a plurality of error detection signals by providing an EXOR operation to the latch signals; and

a plurality of counters configured to count the error detection signals in synchronization with the test clock.